ADC Utilizing Low Area Asynchronous Counter

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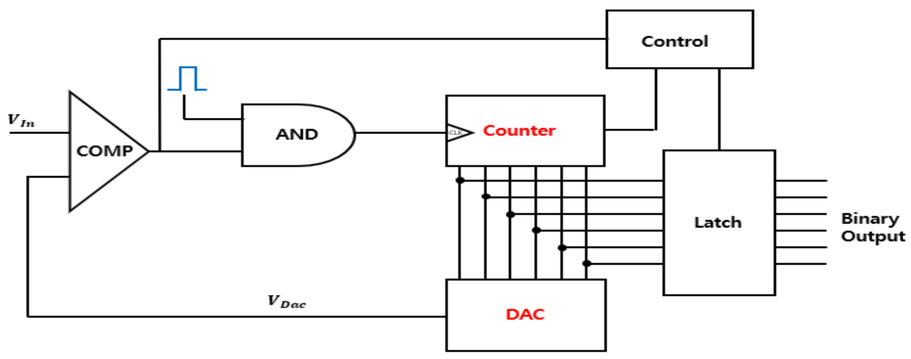
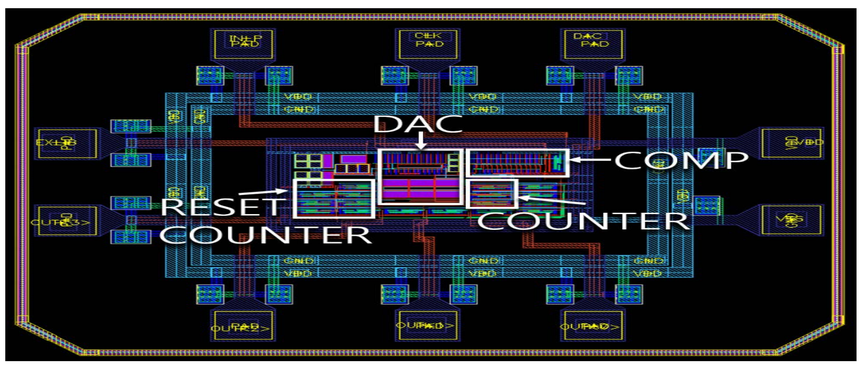
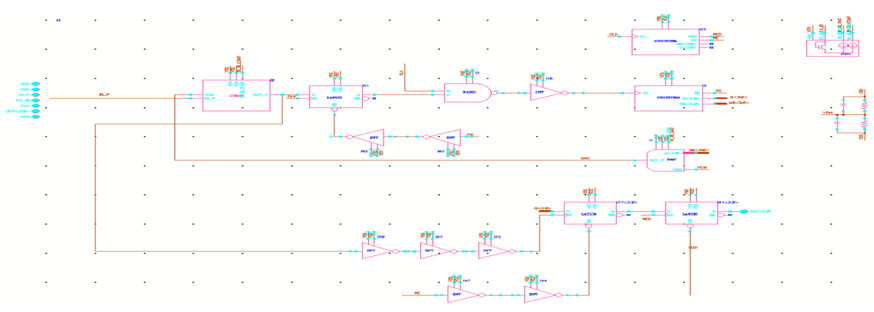
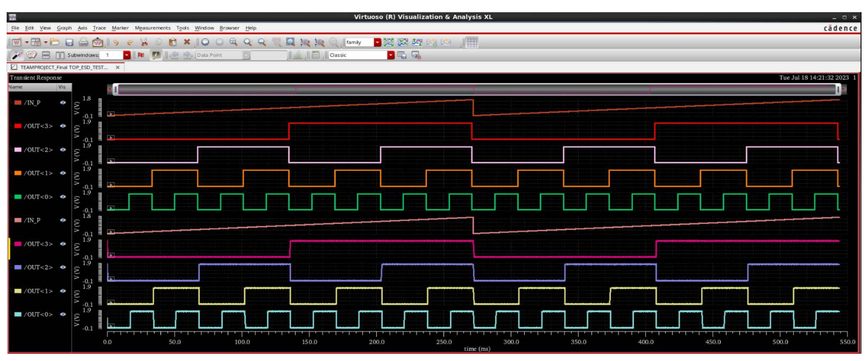
The Counter ADC uses a comparator to store the value of the instantaneous counter where the R-2R DAC output exceeds the analog input voltage in Latch and converts the analog signal into digital code. In this paper, we designed R-2R DAC to receive input signals in discrete time using Two-stage Operational Amplifier, and designed a comparator to compare the input voltage with the step ramp wave output of R-2R DAC. An output buffer is synchronized with a Reset signal so that the sampling frequency becomes constant. In addition, asynchronous counters were used to reduce the area, and Timing Control was performed using Inverter-based Delay Cell to compensate for timing errors caused by delays. Finally, Counter ADC was designed and manufactured using the above circuit.

Schematic & Layout



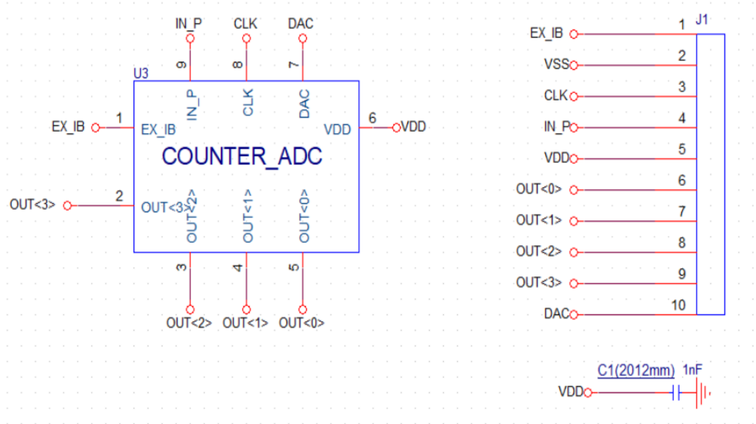




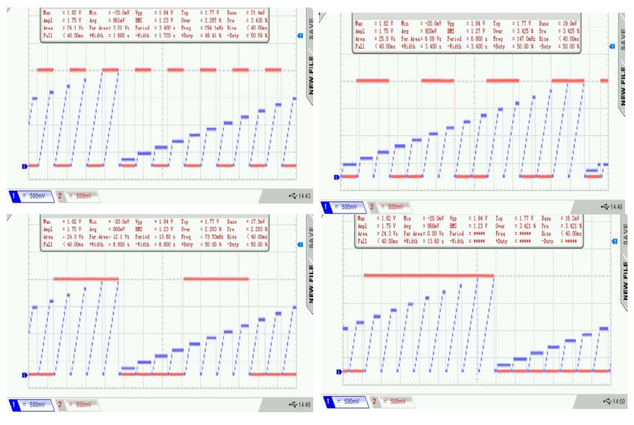


- Compare the analog input to the R-2R DAC step waveform, divide it into 4 bits from 0 to 1.8V and convert it to a digital code (0000 to 1111)
- Counter ADC consists of DAC, Latch, Comparator, Control Logic, and Counter as shown in the figure. The input signal (Vin) and the step signal of the DAC are compared by a comparator, and if the input signal is greater than the step signal, a high (1) value is output, and if the input signal is smaller than the step signal, a low (0) value is output. At this time, the number of clocks counted just before the low (0) value is displayed as a 4-bit digital output.

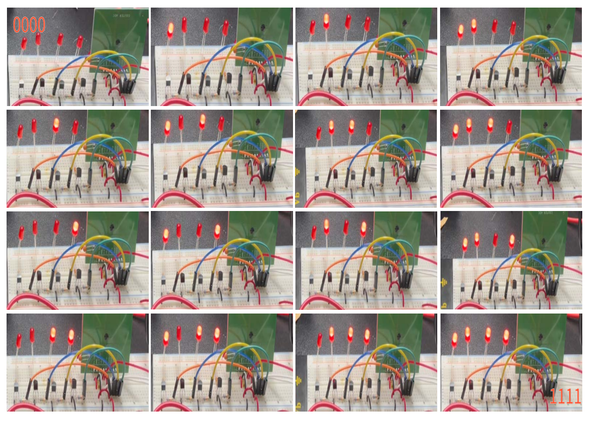
Chip on Board & Chip Test



<PCB>



<Chip Test 1>



<Chip Test 2>

- As MPW does not support packaging, Orcad Schematic and bonding diagram were created to produce CoB.
- Chip Test 1 is measured using an oscilloscope, function generator, and power supply.
- Chip Test 2 uses the above devices, LED, and BJT to construct a circuit to check the output of the Counter ADC.

The Counter ADC was designed and built using Cadence's Spectre and Virtuoso Tool along with DB Hitek's 180nm BCDMOS process. The chip size is 830um x 700um, and the power supply is 1.8V. we were able to design a more stable circuit by giving two-stage Operational Amplifier a PMOS input instead of an NMOS input. The OP Amp DC gain is 92.0704 dB and Unity gain bandwidth is 18.0322 MHz.

Counter ADC is very accurate, and you can increase the accuracy by increasing the number of bits. However, timing control due to asynchronous counter delay is difficult. Therefore, this can be supplemented by using synchronous counters rather than asynchronous counters. The reason why asynchronous counters were used in this paper is easier to implement than synchronous counters. Each Flip-Flop uses a separate Clock, making circuit design simple and intuitive. It is also a relatively small area. We used Inverter-based Delay Cell for Timing Control.

The 4-bit Counter ADC in this paper is simple, easy to expand channels, and can be applied in various fields of overall video signal processing.

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